A PROGRAMMABLE LOGIC DEVICE WITH TIME-MULTIPLEXED INTERCONNECT

This application is a DIV of 10/253,740 filed 09/23/02, now U.S. Pat. 6,829,756.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates generally to programmable logic devices, and in particular to a system and method for time multiplexing the programmable interconnect of a field programmable gate array.

Description of the Related Art

[0002] Programmable logic devices such as field programmable gate arrays ("FPGAs") are a well-known type of integrated circuit and are of wide applicability due to the flexibility provided by their reprogrammable nature. An FPGA typically includes an array of configurable logic blocks (CLBs) that are programmably interconnected to each other to provide logic functions desired by a user (a circuit designer). An FPGA typically includes a regular array of identical CLBs, wherein each CLB is individually programmed to perform any one of a number of different logic functions. These functions may include logic in lookup tables (LUTs) and storage in flip-flops or latches. The FPGA may also include tri-state buffers that users may use to share routing wires. The FPGA has a configurable routing structure called a programmable interconnect (hereinafter interconnect) for interconnecting the CLBs according to the desired user circuit design. The FPGA also includes a number of configuration memory cells which are operatively coupled to the CLBs to specify the function to be performed by each CLB, as well as to the interconnect to specify the coupling of the input and output lines of each CLB.

[0003] One approach available in the prior art to increase the functionality of logic circuits has been increasing the number of CLBs and interconnect structures in the FPGA.